IN THE DRAWINGS:

Please replace the label "Conventional System" with the label "Prior Art," as illustrated in amended FIGs. 1-9.

IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered). Please AMEND claims * and ADD new claims * in accordance with the following:

Please amend claim 13 in accordance with the following:

1. (previously presented) A method for instruction processing executing on a computer, comprising:

identifying a classification of a functional unit which can execute a basic instruction; determining whether said basic instruction can be assigned to a logical instruction slot through checking a relationship between said classification of said functional unit and said logical instruction slot: and

assigning, to an instruction slot, said basic instruction determined to be assignable to said logical instruction slot.

2. (previously presented) The method for instruction processing as claimed in claim 1, wherein said identifying is divided into identifying an instruction category of a basic instruction, and identifying a classification of a functional unit which can execute said instruction category.

3. (previously presented) The method for instruction processing as claimed in claim 1, further comprising prior to said assigning, checking a relationship between said basic instruction that can be assigned to said logical instruction slot and other basic instructions to be assigned to other logical instruction slots.

4. (previously presented) The method for instruction processing as claimed in claim 2, further comprising, prior to said assigning, for checking a relationship between said basic instruction that can be assigned to said logical instruction slot and other basic instructions to be assigned to other logical instruction slots.

5. (previously presented) The method for instruction processing as claimed in claim 3, wherein said determining includes a step of identifying said logical instruction slot having a lowest numeral determined to be assignable.

6. (previously presented) The method for instruction processing as claimed in claim 4, wherein said assigning includes identifying said logical instruction slot having a lowest numeral determined to be assignable.

7. (previously presented) The method for instruction processing as claimed in claim 3, wherein said identifying, determining, checking and assigning are repeated for all instruction slots.

8. (previously presented) The method for instruction processing as claimed in claim 4, wherein said identifying, determining, checking and assigning are repeated for all instruction slots.

9. (previously presented) A computer program executing on a computer and stored on a computer readable medium, comprising:

identifying a classification of a functional unit which can execute a basic instruction; determining whether said basic instruction can be assigned to a logical instruction slot through checking a relationship between said classification of said functional unit and said logical instruction slot: and

assigning, to an instruction slot, said basic instruction determined to be assignable to said logical instruction slot.

10. (previously presented) A computer program as claimed in claim 9, wherein said identifying is divided into identifying an instruction category of a basic instruction, and identifying a classification of a functional unit which can execute said instruction category.

11. (previously presented) The computer program as claimed in claim 9, further comprising , prior to said assigning, for checking a relationship between said basic instruction than can be assigned to said logical instruction slot and other basic instructions to be assigned to other logical instruction slots.

12. (previously presented) The computer program as claimed in claim 10, further comprising, prior to said assigning , for checking a relationship between said basic instruction that can be assigned to said logical instruction slot and other basic instructions to be assigned to other logical instruction slots.

13. (currently amended) A method for aiding instruction processing, comprising: arranging, via computer, variable-length instructions to be executed in an order in a logical instruction slot; and
verifying an arrangement of the variable-length instructions.

REMARKS

On page 2 of the Office Action, the Examiner required Applicants to submit replacement drawing sheets. Applicants have amended the drawings and submit herewith replacement drawing sheets for FIGs. 1-9. In particular, Applicants have replaced the label "Conventional System" with the label "Prior Art," as illustrated in the drawings.

On page 3 of the Office Action, claim 13 was rejected under 35 U.S.C. § 101 due to the claimed invention allegedly being directed to non-statutory subject matter. According to the Examiner, the claimed invention is not tangible and is deemed to be an abstract idea. Applicants have amended claim 13 to include the recitation, "via a computer."

In the Office Action, the Examiner rejected claims "1-15" under 35 U.S.C. § 103(a) as being unpatentable over U.S. Pat. No. 5,640,588 (Vegesna) in view of "Admitted Prior Art as Disclosed in the Background of Invention Section of the Specification." *See* Office Action, page 3. Applicants respectfully request that the Examiner note that there are only thirteen (13) claims in the application.

Vegesna is directed to an apparatus and method for scheduling a sequence of instructions for achieving multiple executions with a Central Processing Unit (CPU). According to Vegesna, an Instruction Buffer Control Register (IBCR) is provided and contains an Instruction Buffer Enable (IBE) at bit zero and a Flush Trap Disable (FTD) at bit one. The IBE permits accesses of an Instruction Buffer (IBUF) 10 by IFETCH 4 when set to a value of one. The IBE disables IBUF 10 when cleared. *See* Vegesna, column 20, lines 20-27. *See also* Vegesna, FIG. 18.

The background section of the specification of the present invention discloses a configuration of a conventional processor based on a very long instruction word architecture. The conventional processor includes a memory, an instruction read unit and instruction registers, as illustrated in FIG. 1. The instruction read unit reads a memory area storing a Very Long Instruction Word (VLIW) instruction addressed by an address stored in a program counter (PC) and writes the VLIW instruction to the instruction register 12. The instruction registers in the conventional system include a number of actual, physical instruction slots (for example, instruction slot 0, instruction slot 1, instruction slot 2, instruction slot 3, instruction slot 4, and instruction slot 5, as illustrated in FIG. 1).

Fig. 4 of Applicants' specification is a flow chart of a conventional assembler, that is, the

assembler utilized in conjunction with Fig. 1, for a VLIW processor. Fig. 5 of Applicants' specification is a flow chart of the VLIW verification operation of Fig. 4. The VLIW verification operation S13 in Fig. 4 includes an instruction slot assignment verification operation S13-1 for fixed length VLIW and a register conflict verification operation S13-2.

The present invention is directed to a method of verifying an arrangement of basic Very Long Instruction Word (VLIW) instructions for language processing systems used on processors designed by variable length VLIW architecture. In at least one embodiment, in the method of the present invention, a determination is made regarding whether a basic instruction can be assigned to a logical instruction slot. In at least one embodiment, a logical instruction slot is a virtual instruction slot which corresponds to a particular functional unit and can be used to store variable length Very Long Instruction Words (VLIW's). *See* Specification of the Present Invention, page 28, lines 6-12.

On page 6 of the current Office Action, in the "Examiner's Response" section, the Examiner indicated that Vegesna does not explicitly teach a logical instruction slot. The Examiner, however, alleges that "APA" (Applicants' Admitted Prior Art) teaches a logical instruction slot and "a third step of assigning, to an instruction slot, said basic instruction determined to be assignable to said logical instruction slot."

As shown in Figure 18, Vegesna simply includes an actual register. In particular, Vegesna discloses an Instruction Buffer (IBUFF) 10, to which access is controlled via an Instruction Buffer Enable (IBE) by an IFETCH 4. *See* Vegesna, column 20, lines 20-25. Therefore, in contrast to the present invention, Vegesna does not disclose or suggest a logical instruction slot. Rather Vegesna discloses an actual physical instruction slot, namely the IBUFF 10.

Contrary to the Examiner's assertion that Applicants have admitted to teachings of a logical instruction slot in the background section of Applicants' specification, Applicants do not believe that the section discloses a logical instruction slot.

On page 7 of the Office Action, the Examiner alleges that the background section discloses, "assigning, to an instruction slot, said basic instruction determined to be assignable to said logical instruction slot," as identified by the language of claim 1, for example. The Examiner cites Figure 5 for support for the allegation. Although operation S13-1 verifies whether each basic instruction of a Very Long Instruction Word instruction is assigned to an instruction slot which can execute the basic instruction, the instruction slots are not virtual instruction slots but rather actual physical instruction slots, as illustrated in Fig. 1. The specification clearly indicates

that Figures 2, 3, and 4 are based on the conventional system illustrated in Figure 1.

Independent claims 1, 9, and 13 are patentable over the references, as neither Vegesna nor Applicants' background section, taken alone or in combination, teaches or suggests the above-identified feature of the present invention. As dependent claims 2-8 and 10-12 depend from independent claims 1 and 9, respectively, the dependent claims are patentable over the references for at least the reasons presented above for the independent claims.

If there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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